Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	137	(reset\$3 near3 (second adj1 (cpu or processor or microprocessor)))	US-PGPUB; USPAT	OR	OFF	2004/12/13 09:52
L2	2	("5870602").URPN.	USPAT	OR	OFF	2004/12/13 09:59
L4	13	(disabl\$3 near6 clock) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/12/13 11:02
L5	3	("5375247"   "5696979"   "6118384").PN. OR ("6400195"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/12/13 10:14
L6	32	(stop\$3 near6 clock) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/12/13 11:02
S1	1	"4368514".pn.	US-PGPUB; USPAT	OR	OFF	2004/12/13 09:52
S2	270	(first or second) adj1 (processor or cpu) with (shar\$3 near3 (RAM or memory))	US-PGPUB; USPAT	OR	OFF	2004/05/26 16:08
S3	4	((first or second) adj1 (processor or cpu) with (shar\$3 near3 (RAM or memory))) with clock\$1	US-PGPUB; USPAT	OR	OFF	2004/05/26 16:07
S4	37	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with synchronous\$4	US-PGPUB; USPAT	OR	OFF	2004/05/27 15:23
S5	2	(((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory))) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with synchronous\$4)	US-PGPUB; USPAT	OR	OFF	2004/05/26 16:16
S6	43	(clock near3 generat\$3) with (multiprocessor)	US-PGPUB; USPAT	OR	OFF	2004/05/26 16:16
<b>S</b> 7	50	(clock near3 generat\$3) with (multiprocessor or multi-processor)	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:06
S8	50	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with phase	US-PGPUB; USPAT	OR	OFF	2004/05/27 14:35
S9	45	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (RAM or memory) with clock\$1	US-PGPUB; USPAT	OR	OFF	2004/05/27 15:46
S10	513	(memory adj1 array) with (memory adj1 controller)	US-PGPUB; USPAT	OR	OFF	2004/05/27 15:52

S11	123	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:16
S12	1	((memory adj1 array) with (memory adj1 controller)) same (multi-processor or (multi adj1 processor))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:17
S13		((memory adj1 array) with (memory adj1 controller)) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory)))	US-PGPUB; USPAT	OR	OFF	2004/05/27 15:52
S14	1038	(memory adj1 array) same (memory adj1 controller)	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:03
S15	2	((memory adj1 array) same (memory adj1 controller)) and (((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (shar\$3 near3 (RAM or memory)))	US-PGPUB; USPAT	OR	OFF	2004/05/27 15:52
S16	581	(memory adj1 array) same (memory adj1 controller) same address\$2	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:03
S17	14	((memory adj1 array) same (memory adj1 controller) same address\$2) and ((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:03
S18	3	((first) adj1 (processor or cpu) with (second) adj1 (processor or cpu)) with (disabl\$3 near3 clock)	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:18
S19	1	(disabl\$3 near3 clock) same (multi-processor or (multi adj1 processor))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:18
S20	9	(disabl\$3 near3 clock) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/12/13 10:13
S21	14	((disabl\$3) with ((first or second) adj1 (processor or cpu))) with clock\$1	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:32
S22	140	(disabl\$3) with ((first or second) adj1 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:40
S23	1937	713/32\$.ccls.	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:40
S24	37	713/32\$.ccls. and ((first adj1 (processor or cpu)) with (second adj1 (processor or cpu)))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:54

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S25	54	713/32\$.ccls. and ((first adj1 (processor or cpu)) same (second adj1 (processor or cpu)))	US-PGPUB; USPAT	OR	OFF	2004/05/27 16:55
S26	16	(713/32\$.ccls. and ((first adj1 (processor or cpu)) same (second adj1 (processor or cpu)))) and (stop\$3 near2 clock\$1)	US-PGPUB; USPAT	ÓR	OFF	2004/05/27 17:00
S27	8307	multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:10
S28	783	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (control\$3 near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:08
S29	302	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:05
S30	202	((multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (control\$3 near2 clock\$1)) and ((multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 clock\$1))	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:04
S31	98	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 (clock\$1 near2 (output\$1 or signal\$1)))	US-PGPUB; USPAT	OR .	OFF	2004/05/27 17:05
S32	23	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((stop\$3 or disabl\$3 or inhibit\$3) near2 (clock\$1 near2 (output\$1)))	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:05
S33	817	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (generat\$3 near2 clock\$1)	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:08
S34	111	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (selective\$3 near2 disabl\$3)	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:10

S35	130	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and (selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3))	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:12
S36	42	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3)) with (processor\$1 or cpu\$1))	US-PGPUB; USPAT	OR	OFF	2004/05/27 17:15
S37	25	(multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1)) and ((selective\$3 near2 (disabl\$3 or inhibit\$3 or stop\$3)) with (clock\$1))	US-PGPUB; USPAT	OR	OFF	2004/05/28 17:36
S38	21	suspend\$3 near3 (second adj1 processor)	US-PGPUB; USPAT	OR	OFF	2004/05/28 17:36
S39	3227	external near3 reset	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:06
S40	797	external near3 reset adj1 signal\$1	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:06
S41	1113	external near3 (reset adj1 signal\$1)	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:10
S42	13	(external near3 (reset adj1 signal\$1)) and (multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1))	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:10
S43	0	(external near3 (reset adj1 signal\$1)) and (multi-processor or (multi adj1 processor) or dual-processor\$2 or (dual adj1 processor\$1))	EPO; JPO; IBM_TDB	OR	OFF	2004/05/28 18:10
S44	185	external near3 (reset adj1 signal\$1)	EPO; JPO; IBM_TDB	OR	OFF	2004/05/28 18:10
S45	0	first adj1 (external near3 (reset adj1 signal\$1))	EPO; JPO; IBM_TDB	OR	OFF	2004/05/28 18:10
S46	17	first adj1 (external near3 (reset adj1 signal\$1))	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:25
S47	207	(high adj2 (processor or cpu)) with (low adj2 (processor or cpu))	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:26
S48	9	((high adj2 (processor or cpu)) with (low adj2 (processor or cpu))) and 713/32\$.ccls.	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:49
S49	3	"6240521".URPN.	USPAT	OR	OFF	2004/05/28 18:29
S50	13	(first or second) adj1 external adj1 reset	US-PGPUB; USPAT	OR	OFF	2004/05/28 18:49

S51	1	"973888"	US-PGPUB	OR	OFF	2004/06/02 13:38
S52	1	"5903503".pn.	USPAT	OR	OFF	2004/06/02 10:27
S53	5	(phase near2 synchroni\$7) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2004/11/15 17:29
S54	15	"5631591".URPN.	USPAT	OR	OFF	2004/11/15 17:21
S55	0	(phase near2 align\$6) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2004/11/15 17:30
S56	78	(phase near2 synchroni\$7) same (memory with (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2004/11/15 17:28
S57	5	(phase\$1 near2 synchroni\$7) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2004/11/15 17:30
S58	0	(phase\$1 near2 align\$6) same (second adj1 (processor or CPU))	US-PGPUB; USPAT	OR	OFF	2004/11/15 17:30
S59	6	"5903747".URPN.	USPAT	OR	OFF	2004/11/15 17:31
S60	10	"5510740".URPN.	USPAT	OR	OFF	2004/11/15 17:33
S61	1	"6118314".URPN.	USPAT	OR	OFF	2004/11/15 17:34